



NASA Electronic Parts and Packaging (NEPP) Program



# **2013 NEPP Tasks Update for Ceramic and Tantalum Capacitors**

**Alexander Teverovsky**

**Parts, Packaging, and Assembly Technologies  
Office, Code 562, GSFC/ Dell Services Federal  
Government, Inc.**

**[Alexander.A.Teverovsky@nasa.gov](mailto:Alexander.A.Teverovsky@nasa.gov)**

# Reliability Assurance for Ceramic and Tantalum Capacitors Tasks

- ❑ Screening techniques for ceramic capacitors with cracks.
  - How to select robust parts and prevent cracking?
  - How cracking affects reliability and performance?
  - What testing would mitigate the risk of failure?

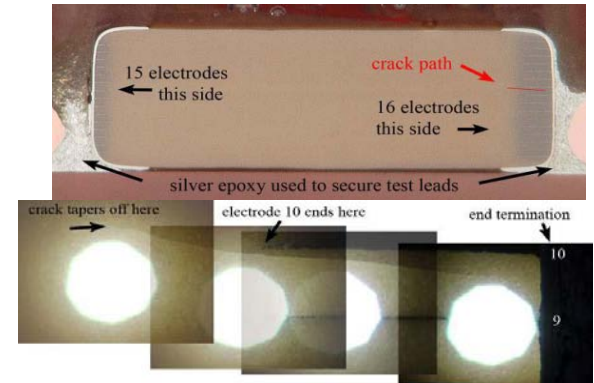
- ❑ Reliability of advanced wet and solid tantalum capacitors.

## Wet capacitors:

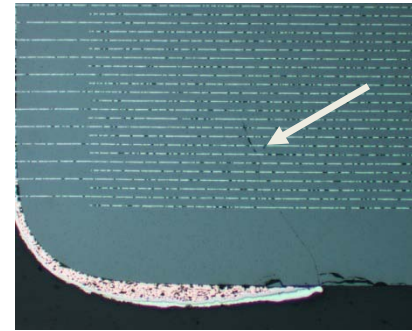
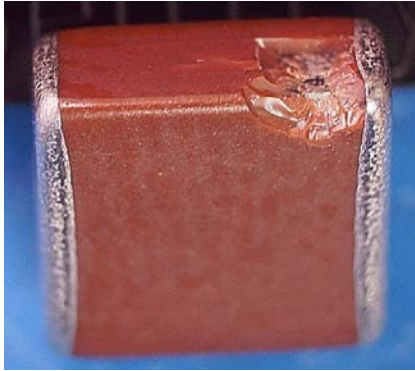
- Effect of reverse bias and requirements for qualification testing.
- Effect of random vibration and requirements for lot acceptance testing.
- Effect of ripple currents and requirements for qualification testing.

## Solid capacitors:

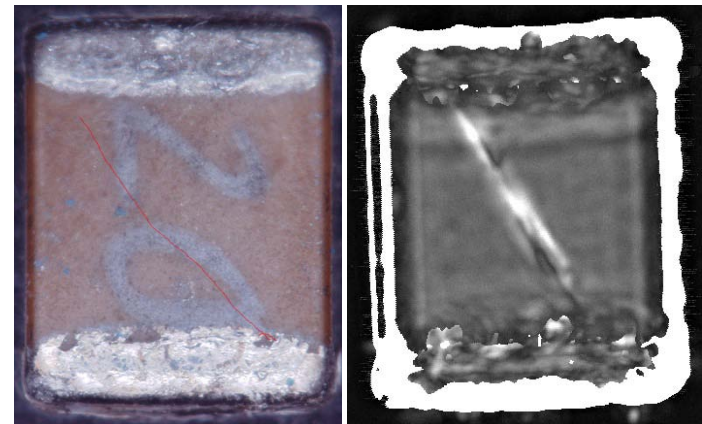
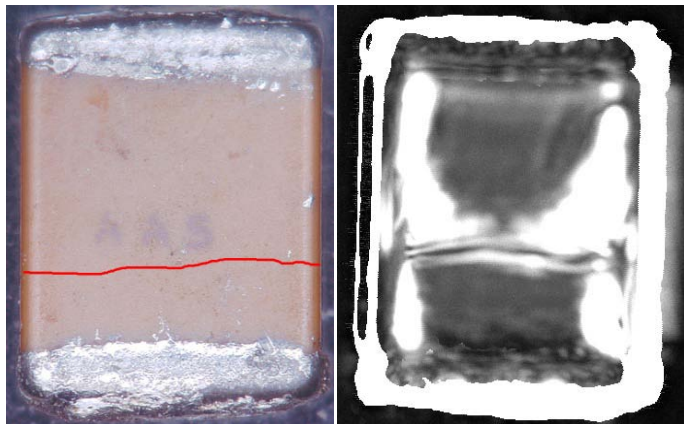
- Surge current testing and requirements for surge-limiting resistors.
- Weibull grading test and voltage derating requirements.



0.1uF 50V MLCC failed after 1.5y of the system operation and testing (FA by C. Greenwell)

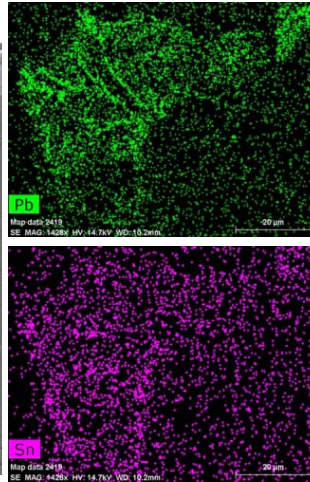
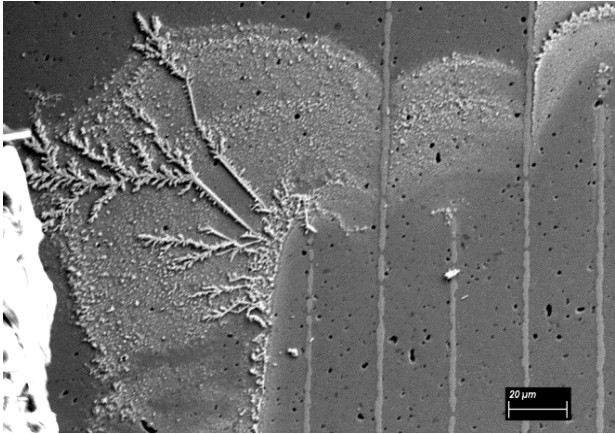


# Testing Techniques for Low-Voltage Ceramic Capacitors with Cracks



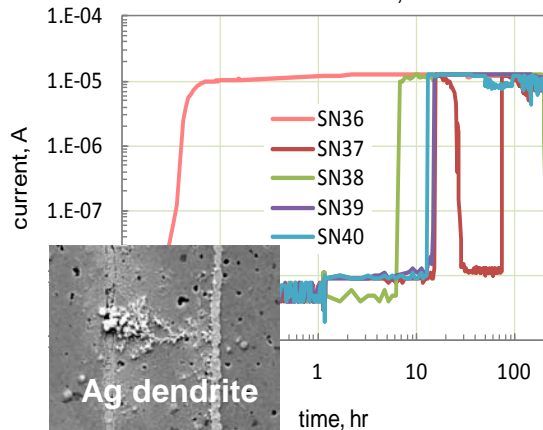
# Effectiveness of Humidity Steady State Low Voltage (HSSLV) Testing

0.47 $\mu$ F 50V PME, WLT at 0.8 V

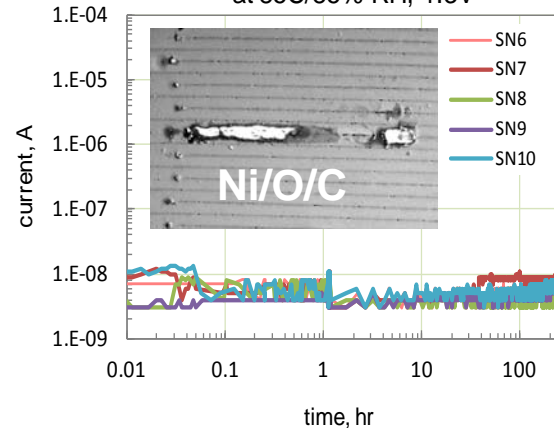


- ❑ Pb and Sn dendrites and deposits are formed near the edge cathode electrodes.
- ❑ HSSLV failures: 0/20 BME, 17/20 PME.
- ❑ Ag dendrites on PME and nickel carbonates on BME.

PME Mfr.C 1825 0.47 $\mu$ F 50V X-sect.  
at 85C/85% RH, 1.3V

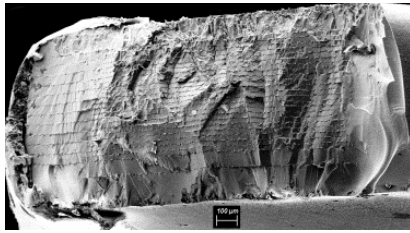


BME Mfr.A 1825 0.47 $\mu$ F 50V X-Sect.  
at 85C/85% RH, 1.3V

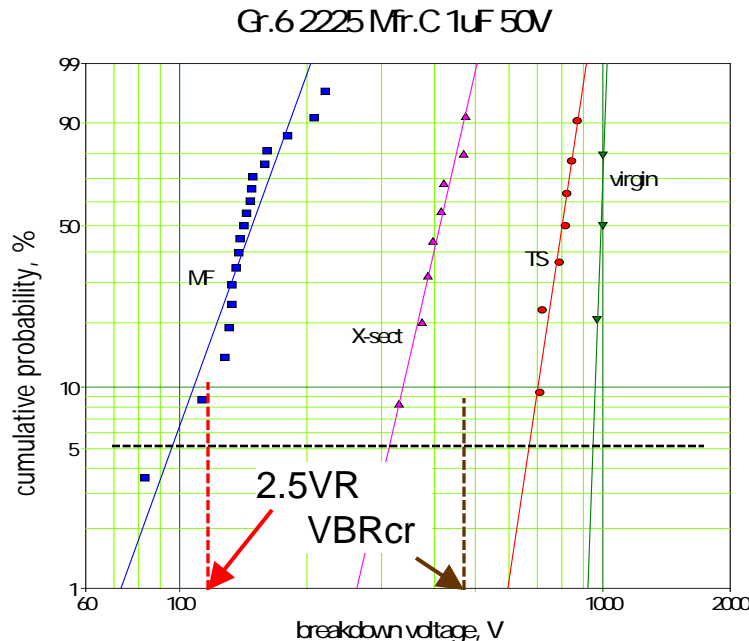


- ✓ HSSLV testing might be useful for PME capacitors but is much less effective for BME capacitors.
- ✓ BMEs are less susceptible to LVF.





# Effectiveness of DWV Test

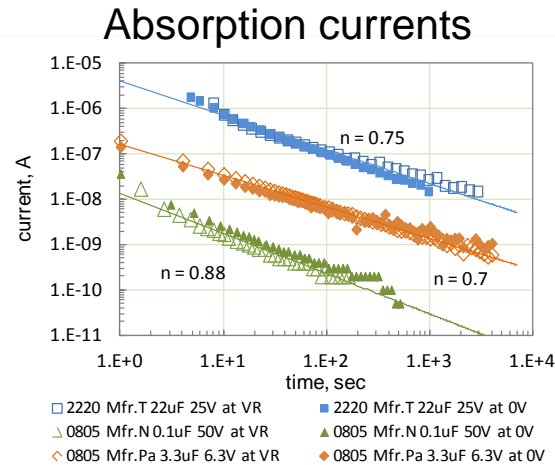
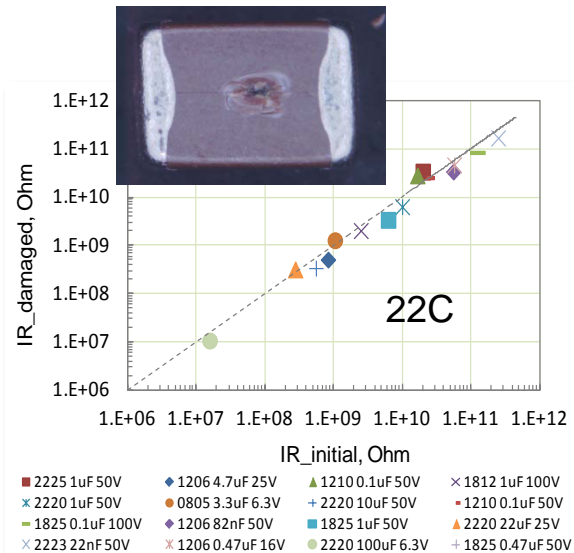


- ❑ Dielectric Withstanding Voltage (DWV) test requires application of 2.5 times rated voltage (VR).
- ❑ Only ~20% of parts with gross defects failed the test.
- ❑ 19 out of 30 (63%) lots of parts damaged by X-sectioning and thermal shock (TS) had the probability of DWV test failure <1%.

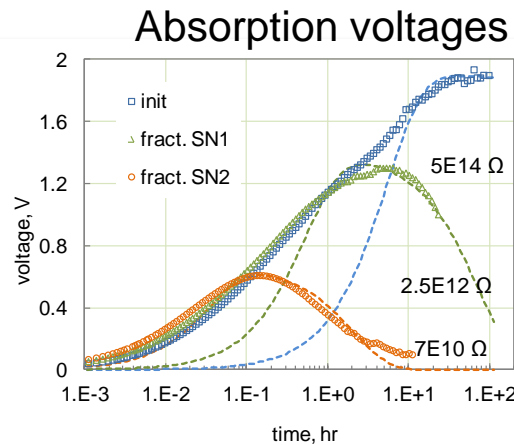
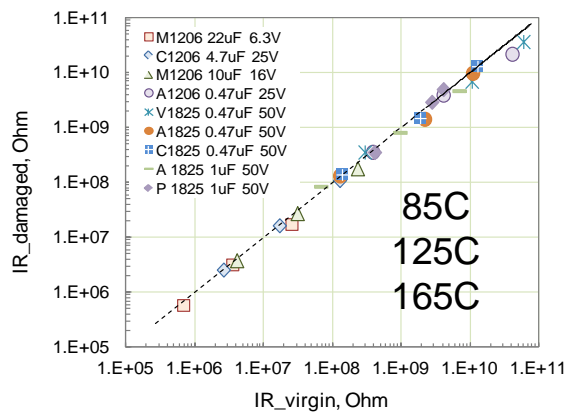
- ✓ Breakdown voltage (VBR) is sensitive to the presence of defects and reflects quality of the lot.
- ✓ The effectiveness of the existing DWV testing is low.
- ✓ Guidelines:  $VBR_{cr} = 0.5 \times (VBR_{avr} - 2 \times \sigma) - (5\% \text{ level})/2$

# Effectiveness of IR measurements

$$I(t, T, V) = I_{abs}(t, V) + I_{il}(T, V) + I_{dl}(t, T, V, RH)$$

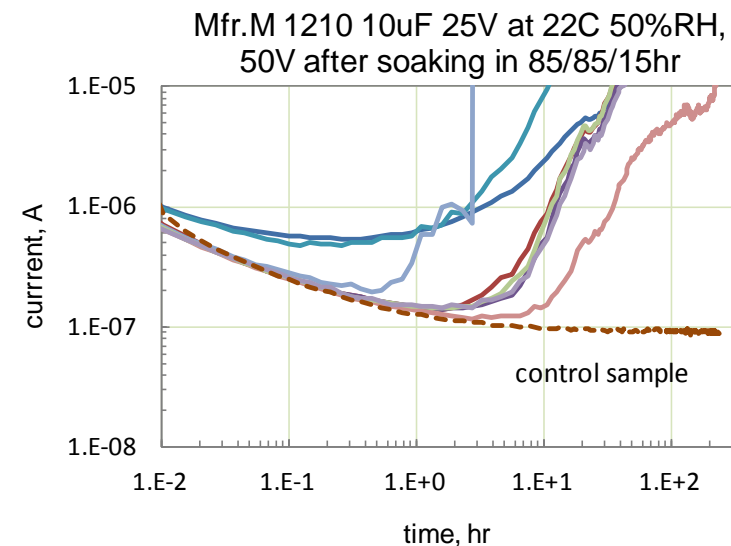
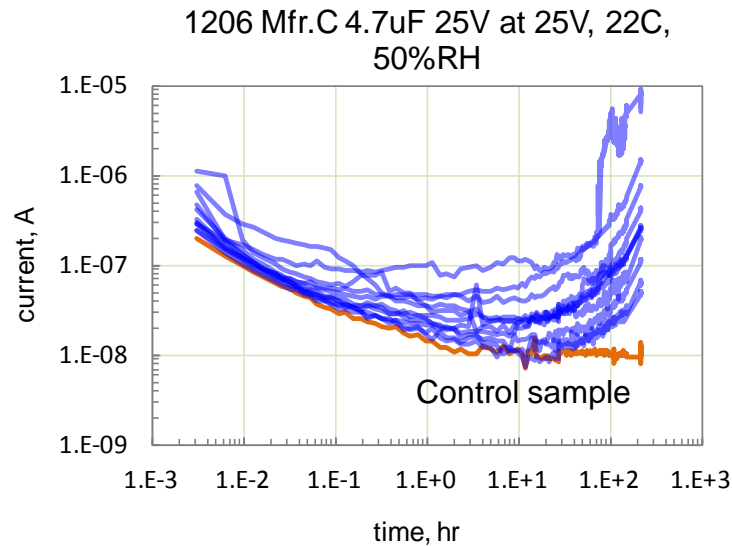


- Absorption currents prevail at room temp.
- Intrinsic leakage currents prevail at high temperatures, >85 °C.



- ✓ Standard IR measurements fail to reveal cracks in BME MLCCs.
- ✓ Measurements of absorption voltages can expose the difference.

# Degradation of Leakage Currents in BME MLCCs with Cracks



- ✓ Monitoring of leakage currents with time at VR to 2xVR during or after exposure to humid environments might be a useful technique to reveal capacitors with cracks.
- ✓ The effectiveness of the Resistance to Moisture Absorption Test (RMAT) is currently being evaluated.

# Guidelines for Commercial Ceramic Capacitors

- ❑ Guidelines, Rev.A, that addresses issues related to both, PME and BME capacitors, has been posted at the NEPP web site in 2012.

- I. *Scope*
- II. *Background*
- III. *Parts selection and construction analysis/DPA*
- IV. *Lot acceptance testing*
- V. *Qualification testing*
- VI. *Freshness policy*
- VII. *Derating*
- VIII. *Assembly*



NASA Electronic Parts and Packaging  
(NEPP) Program



NEPP Task:

Screening Techniques for Ceramic Capacitors

**Guidelines for Selection, Screening and  
Qualification of Low-Voltage  
Commercial Multilayer Ceramic  
Capacitors for Space Programs**

Rev. A

Alexander Teverovsky

Dell Perot Systems  
Code 562, NASA GSFC, Greenbelt, MD 20771  
[Alexander.A.Teverovsky@nasa.gov](mailto:Alexander.A.Teverovsky@nasa.gov)

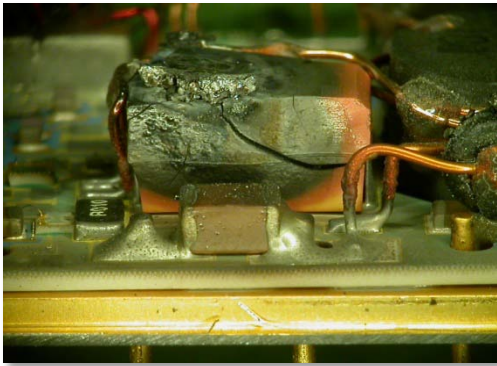
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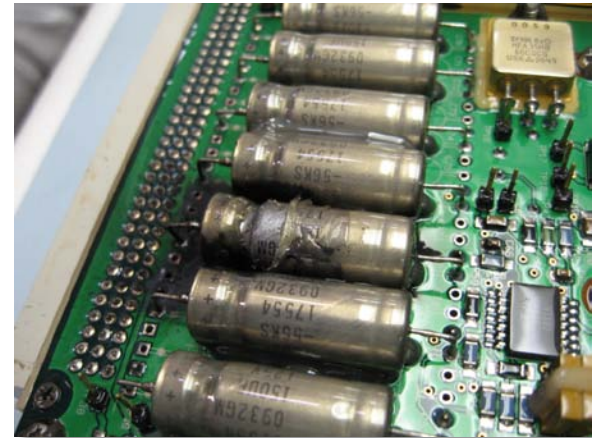
- ✓ Rev.B of the guidelines that addresses cracking-related issues in more details will be prepared in 2014.







# Reliability of Advanced Wet and Solid Tantalum Capacitors



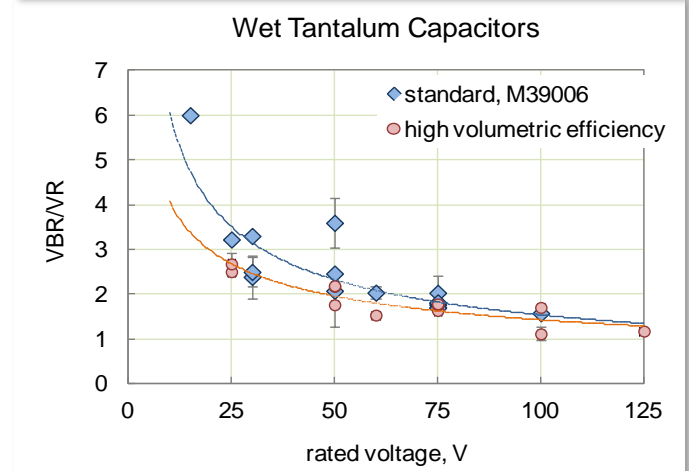
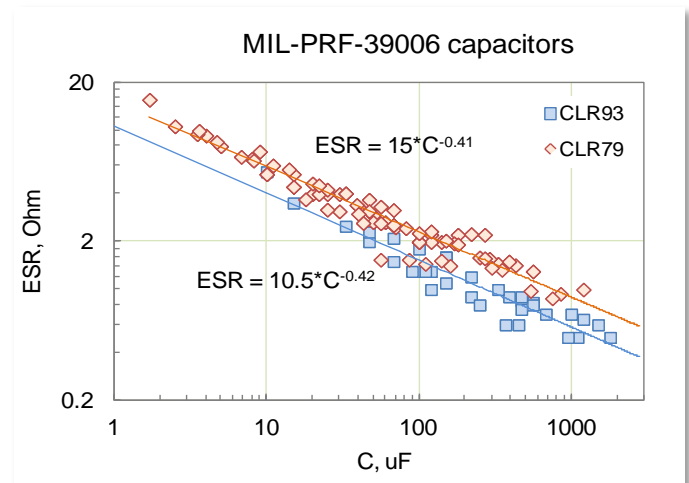
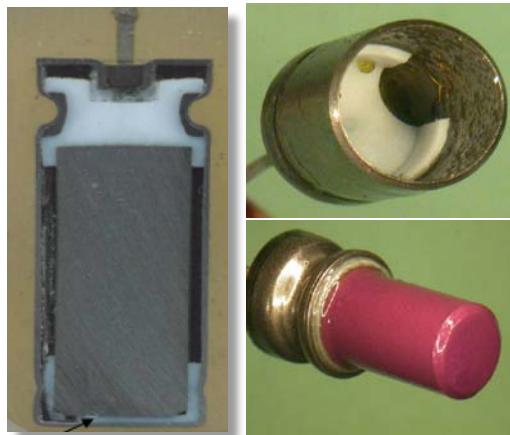
# High Volumetric Efficiency Capacitors

- ❑ Volumetric efficiency is achieved by reducing the thickness of the cathode layer, increasing the size of the slug, and using high-CV powders.

M39006

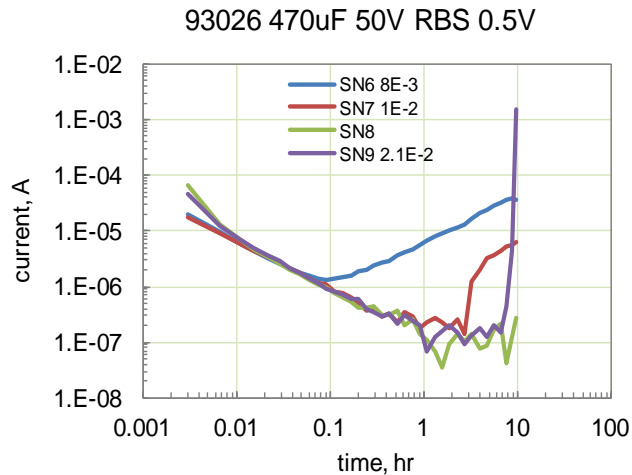


DWG93026



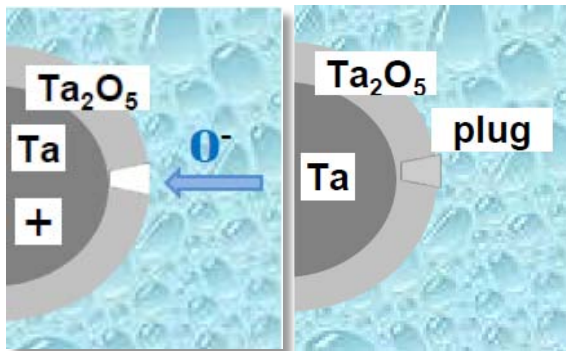
- ✓ Breakdown margin is similar for both types of capacitors.
- ✓ Anodic system remains the same => no effect on life testing.
- ✓ Better performance does not come free: effect of design on reliability at reverse bias and vibration.

# Effect of Reverse Bias (RB)

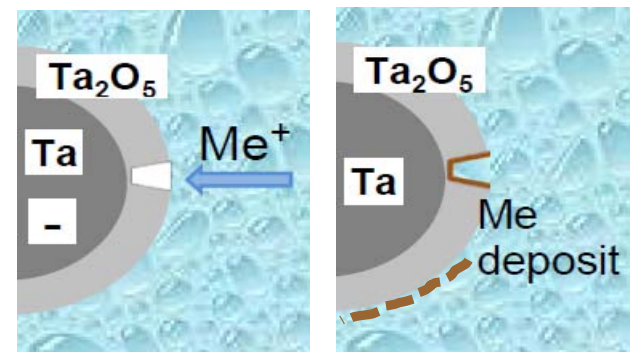
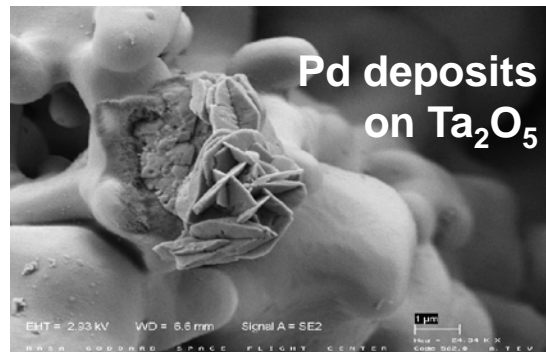


- ❑ The transfer charge to failure is below the specified value of 0.05C.
- ❑ Failures result in increasing leakage currents, bulging of the case, electrolyte leak, and corrosion.
- ❑ Failures might occur at  $RB < 0.5$  V.
- ❑ Some part types can withstand long-term reverse bias at 1.5V.

Forward bias: Oxidation



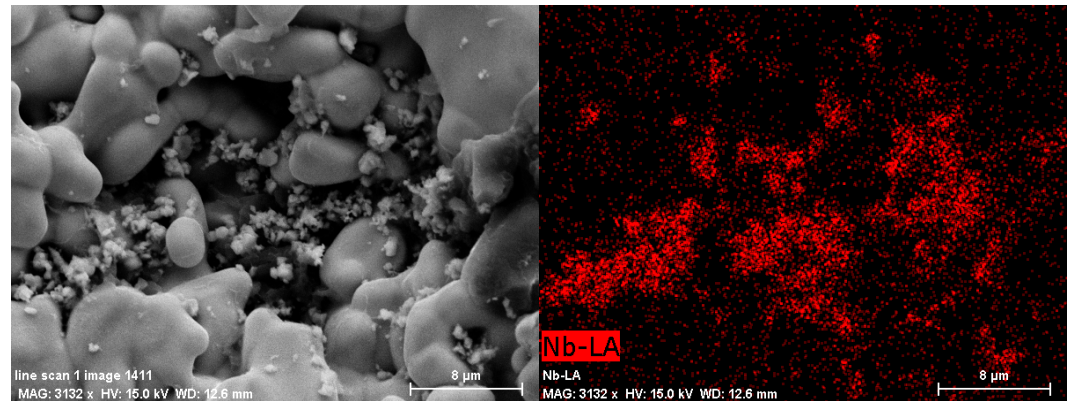
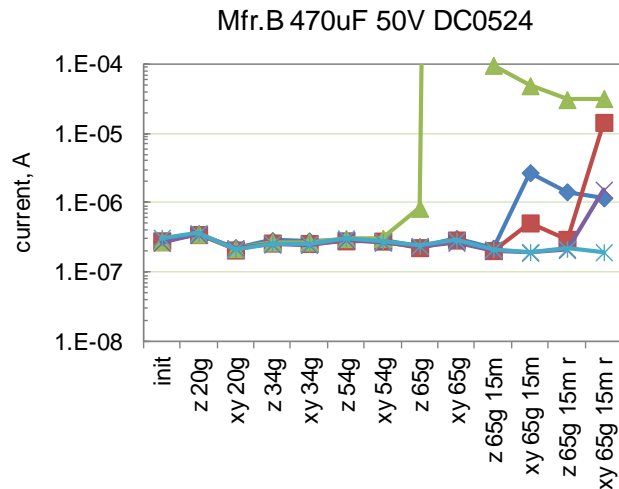
Reverse bias: Electrodeposition of cathode Me



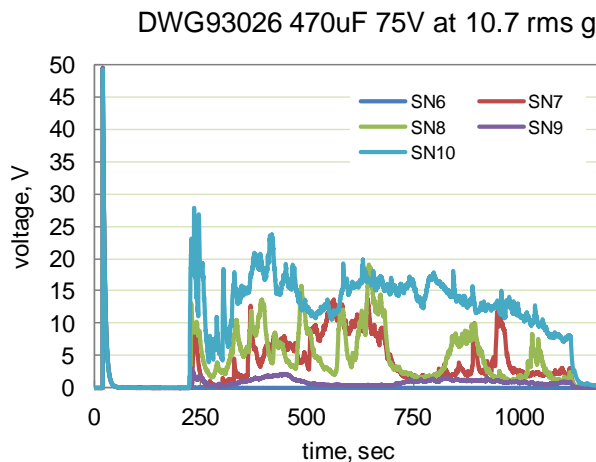
# Effect of Vibration

- ❑ Capacitors are qualified to 20 g sin high frequency vibration only.

Failures due to NbO particles inside the slug

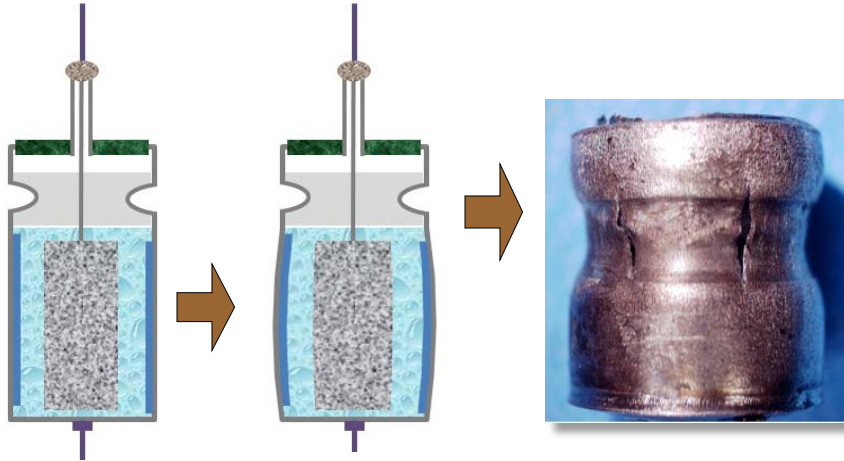


- ✓ Different part types have failures from 10 g<sub>rms</sub> to > 65 g<sub>rms</sub>.
- ✓ Some DWG93026 parts can fail at vibration levels that are below MAR requirements.
- ✓ New design capacitors are qualified to random vibration at 27.7 g<sub>rms</sub>.



# Mechanism of Failures

H<sub>2</sub> generation at cathode:  
 $2e^- + 2H_2O(L) \Rightarrow H_2(g) + 2OH^-(aq)$

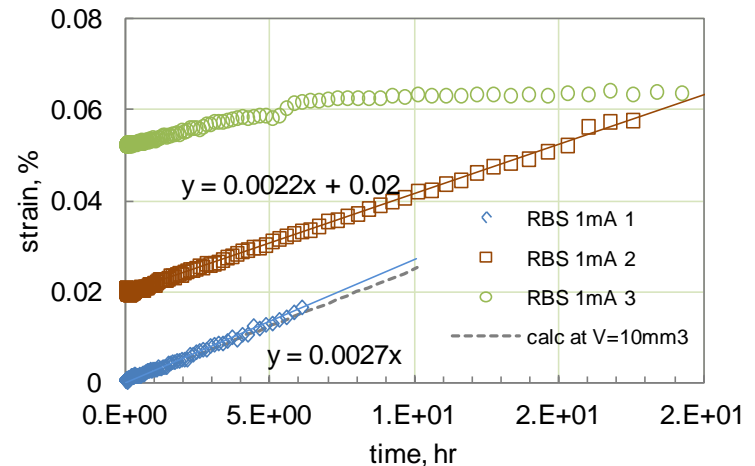


$$n = \frac{I \times t}{z \times F} \quad P = n \times \frac{RT}{V} \quad \varepsilon = \frac{P \times r}{E \times h}$$

- ❑ Gas pressure can be calculated using Faraday and gas laws.
- ❑ Strain ~0.07% corresponds to a pressure of dozens of atm.
- ❑ Gas pressure  $\Rightarrow$  H<sub>2</sub> embrittlement at cold work areas  $\Rightarrow$  fracture.
- ✓ Guidelines testing requirements: random vibration at 20 g<sub>rms</sub>, and reverse bias at 85C, 1.5V.

Case deformation measured by flexible gages

DWG93026 470uF 75V RBS 1mA





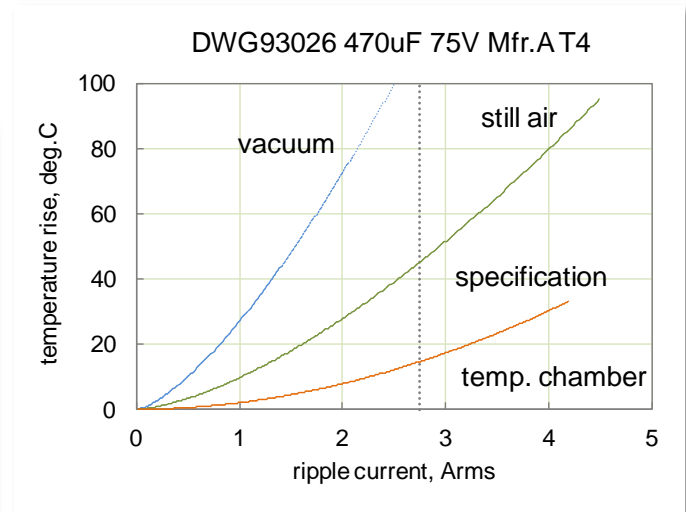
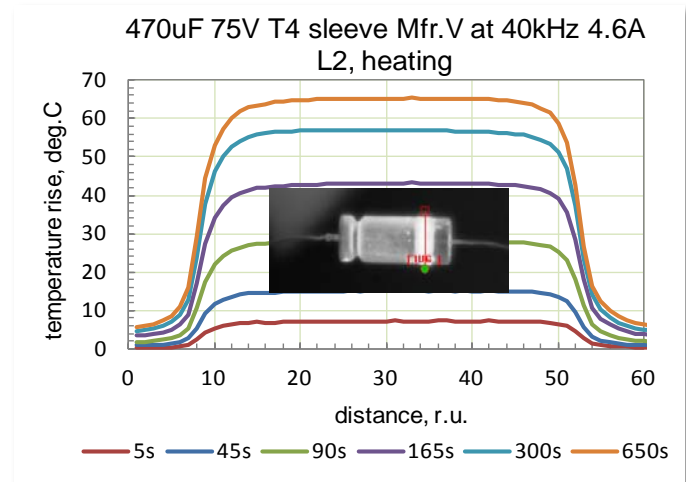
# Ripple Current Testing and Derating

Questions to be addressed:

- How maximum ripple current is determined?
- Is life ripple current testing more stressful compared to the DC bias only life test?
- How vacuum affects temperature rise?
- What ripple currents can be applied at low temperatures, frequencies?
- Do we need to derate ripple currents?

Preliminary results:

- Derating is necessary.
- At  $f < 1$  kHz thermal run-away is possible.
- Ripple life testing is less stressful than regular life testing at 85°C and VR.



# Guidelines for Wet Tantalum Capacitors

- ❑ Guidelines, Rev.A, that addresses reverse bias and vibration testing issues has been posted at the NEPP web site in 2012.

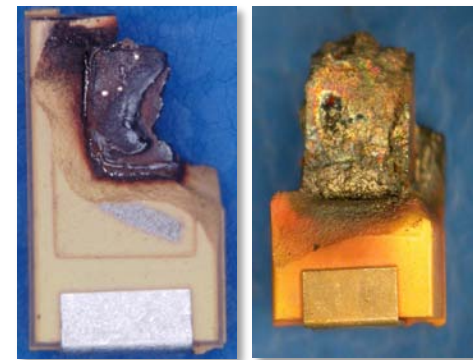
- I. *Scope*
- II. *Background*
- III. *Failure rate*
- IV. *Construction analysis/DPA*
- V. *Lot acceptance testing*
- VI. *Qualification testing*
- VII. *Freshness policy*
- VIII. *Derating*



- ✓ Rev.B of the guidelines that includes requirements for ripple current testing is currently being developed.



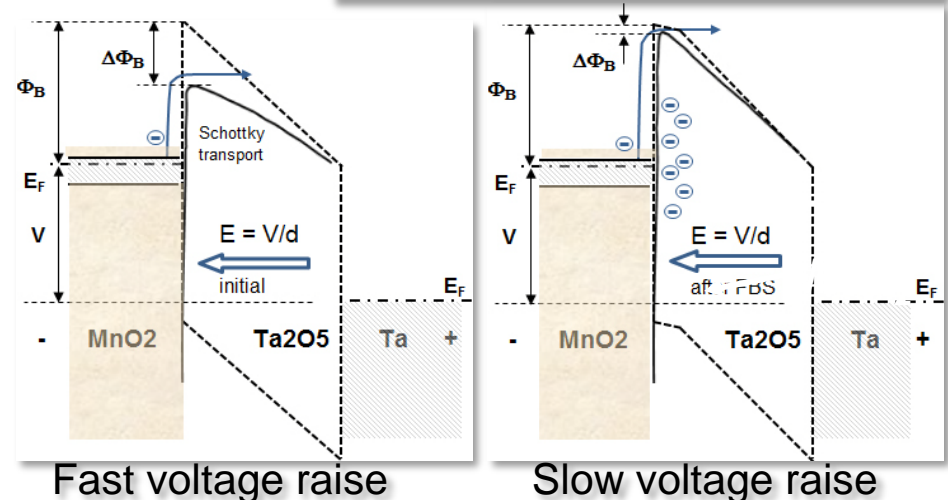
# Surge Current Testing (SCT) and Derating for Solid Tantalum Capacitors



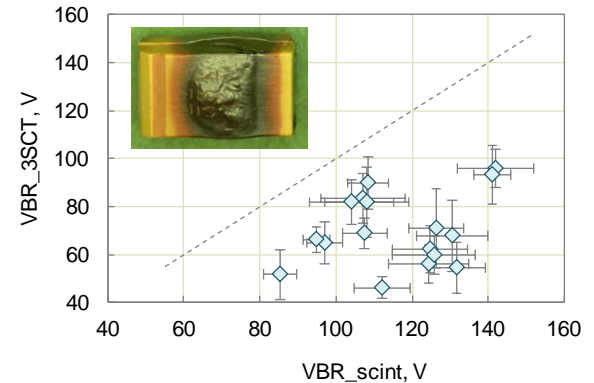
# Effect of $dV/dt$ on Breakdown Voltage

- ❑ Scintillation breakdown voltage,  $VBR_{scint}$  ( $dV/dt \sim 1$  to  $5$  V/sec) is always greater than the surge current breakdown voltage,  $VBR_{surge}$  ( $dV/dt \sim 10^5$  to  $10^6$  V/sec)
- ❑ The rate of voltage increase changes charges and electrical field at the interface.

Accumulation of electrons on traps at the  $MnO_2$ - $Ta_2O_5$  interface with time increases the barrier, the level of electron injection, and the probability of avalanching.



Effect of  $dV/dt$  on VBR for 50V capacitors



- ✓ The rate of voltage increase is critical for breakdown.
- ✓ A resistor in series with a capacitor reduces  $dV/dt$  and failures.

# Surge Current Derating Requirements

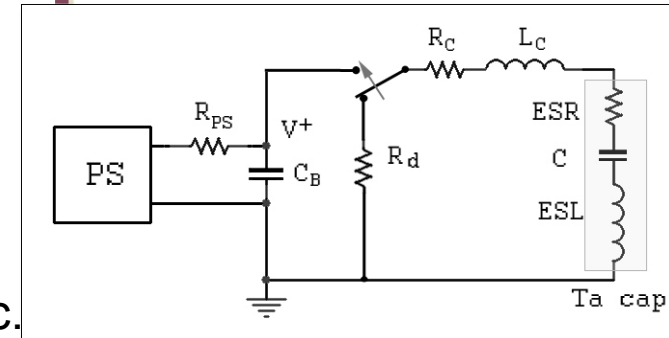
- ❑ History of requirements for circuit resistance ( $R_{ac}$ ):
    - In the 1960s: 3  $\Omega$  per each volt of operating voltage.
    - By the 1980s: 1  $\Omega$  per each volt.
    - From the 1990s: 0.1  $\Omega$  per volt or 1 ohm, whichever is greater.
  - ❑ Manufacturers consider surge current failures as the major reason for voltage derating.
  - ❑ Do we need derating of currents in addition to voltage?
  - ❑ The limit for acceptable surge currents is set by the SCT conditions: the current during applications should not exceed the current during testing:  $I_{appl.} < I_{test}$  “use as tested”
- ✓ Improvements in reliability and the need to increase the efficiency of power supply systems resulted in reduction of  $R_{ac}$ .
  - ✓ At what conditions we can allow circuit designs without  $R_{ac}$ ?
  - ✓ Need a closer look at how the  $I_{test}$  is specified.



# MIL-PRF 55365 SCT Requirements

## ❑ SCT per MIL-PRF-55365H:

- Number of cycles:  $N_c = 4$  surge cycles.
- Energy storage capacitor:  $C_B = 20 \times C_{DUT}$
- Test voltage: VR
- Charge time,  $t_{ch}$ , and discharge time,  $t_{disch}$ ,  $\geq 1$  sec.
- Total DC resistance of the test circuit,  $R_{tc}$ , including the wiring, fixturing, and output impedance of the power supply should not exceed 1  $\Omega$ .
- Measurements after SCT: DCL, C, DF (still no requirements for ESR)
- The minimum surge peak current shall be:  $I_{test} \geq VR / (R_{tc} + ESR_{spec})$ ,  $R_{tc} = 1 \Omega$ .
- Failure condition: current = 1A after 1ms for  $C \leq 330\mu F$ ; 10ms for  $C \leq 3.3mF$ , and 100ms for  $C > 3.3mF$ .



## ❑ Before 12/1/2012:

- $N_c = 10$ .
- $t_{disch} = t_{ch} = 4$  sec.
- $R_C \leq 1.2$  Ohms.
- $C_B \geq 50$  mF.
- No  $I_{test}$  requirements.

- ✓ New specification recognizes the role of *ESR* as a limiting factor for surge currents. However, no specifics for  $I_{test}$  verification.
- ✓ M55365 does not guarantee reliable operation at VR:  $V_{test} = V_{C\_MAX} = 0.95 \times VR$ ,  $\Rightarrow$  the need for voltage derating.

# Application vs. Testing Conditions

## □ Typical application conditions:

- No limiting resistors, minimal inductance.
- Minimal contact resistance.
- Resistance of the circuit,  $R_{ac}$ , is minimal and the current is limited mostly by ESR.

## □ Surge Current Test conditions:

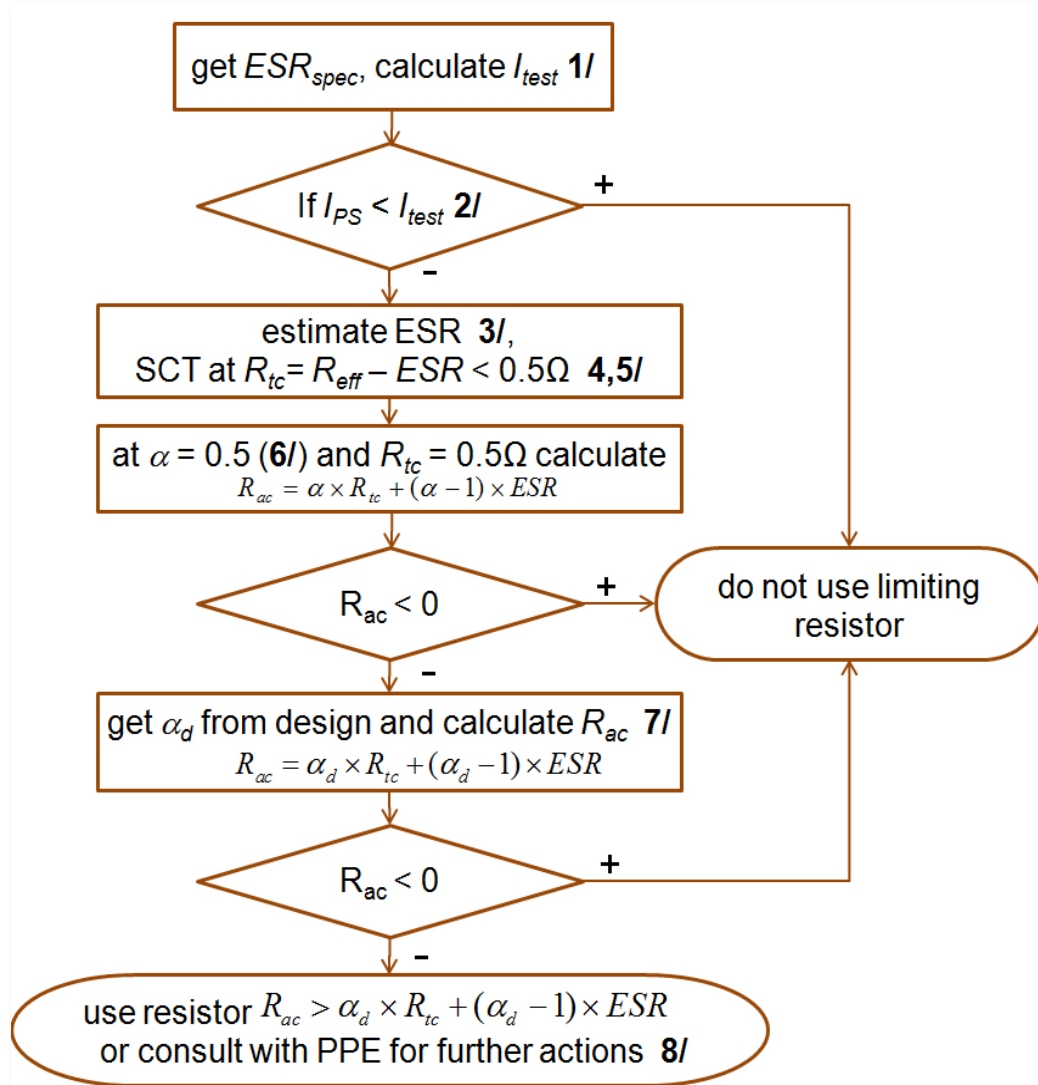
- Unspecified contact resistance of fixtures.
- Limiting resistor can be up to 1  $\Omega$ .
- Relatively long wires and inductance.
- No clear requirements for  $I_{test}$  verification (when, how?).
- Parts with poor contacts in the fixture can pass the testing.

## Example:

- A 15 $\mu$ F 10V CWR06 capacitor with specified ESR=2.5 $\Omega$  and real ESR = 0.5 $\Omega$  is used in a 5V line.
- During application the part can experience a spike:  
$$\underline{I_{appl} = 5/0.5 = 10 \text{ A.}}$$
- During the testing it will be verified to the current:  
$$\underline{I_{test} = 10/(1+2.5) = 2.8 \text{ A}}$$

- ✓ Application conditions might be more severe than test conditions.
- ✓ There is a need in tightening test requirements.

# Algorithm for Surge Current Derating



1/  $I_{test} = \frac{VR}{R_{tc} + ESR_{spec}}$ ,  $R_{tc} = 1 \Omega$

2/ In case of using power supplies (PS) with current compliance, make sure that the clamping time  $\tau \leq 10\mu s$ .  $I_{PS} = I_{max} PS$ .

3/ Estimate ESR as  $ESR_{spec}/N$ , where  $N=7, 3, 2$  for CWR06/11/29 respectively.

4/  $R_{eff} = VR/I_{sp}$ , where  $I_{sp}$  is the surge current spike amplitude.

5/ SCT should be carried out at a min. wire length, no limiting resistors, and  $I_{sp}$  should be verified to be greater than  $I_{sp} > VR/(0.5 + ESR)$

6/ Standard voltage derating:  $\alpha = 0.5$

7/ Actual derating:  $\alpha_d = V_{app}/VR$

8/ Suggestions for further actions:

- experimental data for ESR,
- calculate actual  $R_{tc} = R_{eff} - ESR$ ,
- SCT at greater voltage levels, ...

# Conclusion

- ❑ Testing techniques for ceramic capacitors with cracks:
  - The effectiveness of CSAM, VBR, DVW, IR and HSSLV testing to reveal capacitors with cracks has been evaluated and improvements suggested.
  - Mechanisms of degradation of leakage currents and failures in capacitors with cracks are being studied and rev.B of the guidelines for selection and testing of commercial MLCCs is planned for 2014.
- ❑ Reliability of advanced wet and solid tantalum capacitors.

## Wet capacitors:

- Mechanisms of failures under reverse bias conditions and vibration have been studied and the relevant qualification and lot acceptance tests are suggested.
- There is a need for ripple current testing and derating. A new version of the guidelines will be developed in 2013.

## Solid capacitors:

- Tantalum capacitors manufactured per M55365 might fail in applications due to non-adequate surge current test requirements if used without limiting resistors.
- An algorithm for additional testing that are necessary to assure reliable operation of capacitors without limiting resistors is suggested.